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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant(s): FRERICHS | Confirmation No. 1532 |
| Application No.: 10/524,672 | Art Unit: 2892 |
| Filed: 28 Feb 2007 | |
| Title: METHOD FOR THE PRODUCTION OF A FIXED CONNECTION BETWEEN TWO LAYERS OF A MULTILAYER SYSTEM, AND MULTILAYER SYSTEM | Examiner: GORDON, MATTHEW E |
| Attorney Docket No.: 1001/0165PUS1 | |

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANTS' APPEAL BRIEF

Sir:

A Notice of Appeal was filed in the above application on November 3 2010, with a Request for Pre-Appeal Brief Review. A Notice of Panel Decision from Pre-Appeal Brief Review dated November 24, 2010, indicated that at least one actual issue for appeal was found to exist and that the application should proceed to the Board of Patent Appeals and Interferences. Applicant is filing this Appeal Brief within three months of the date of the Filing of the Notice of Appeal together with a request for Extension of Time and the required fee.

I. REAL PARTY IN INTEREST

The real party in interest in the above-captioned application is MICRONAS GMBH as shown by the assignment recorded at patent Reel 016877, Frame 0581 on

02/24/2011 HMARZI1 00000028 10524672
01 FC:1402 540.00 OP

October 12, 2005.

## II. RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences or judicial proceedings known to the applicant, the applicant's legal representatives or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 16-27 and 32-33 are pending in the above-captioned application with claims 16, and 32 being independent, and the rejection is being appealed.

## IV. STATUS OF AMENDMENTS

No Amendments were submitted subsequent to the Final Rejection of June 3, 2010.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

A) Claim 16

The multilayer semiconductor of independent claim 16 includes a first functional layer 2, a second functional layer 6, an intermediate layer 1 disposed between the first and the second functional layers in a first predetermined region, and a plurality of anchoring elements 9 each embedded in at least two of the first and the second

functional layers, and the intermediate layer, where the anchoring elements comprise a different material 4 than that of the first and the second functional layers (pages 23 and 24 of Clean copy of Specification and Figures 6, 7 and 8).

B) Claim 17

Claim 17 limits claim 16 to where each of the plurality of anchoring elements is embedded in the second functional layer 6 and in the intermediate layer 1 (Figures 6, 7 and 8).

C) Claim 18

Claim 18 limits claim 16 to where a cross-sectional area of each of the plurality of anchoring elements is cylindrical (Figure 8).

D) Claim 19

Claim 19 limits claim 16 to where a cross-sectional area of each of the plurality of anchoring elements 9 increases from one end of the anchoring element to the other end of the anchoring element (Figures 6 and 7).

E) Claim 20

Claim 20 limits claim 16 to where a cross-sectional area of each of the plurality of anchoring elements has a conical shape (Figures 6 and 7).

F) Claim 21

Claim 21 limits claim 16 to where the first 2 and the second functional layers 6 adjoin each other in a second predetermined region that is outside the first predetermined region (Figure 7).

G) Claim 22

Claim 22 limits claim 16 to where the intermediate layer is adhered to the first functional layer (Figures 6-8).

H) Claim 23

Claim 23 limits claim 16 to where a diameter of each of the plurality of anchoring elements lies in a range between 100 and 100 nm (Page 25, lines 5-7).

I) Claim 24

Claim 24 limits claim 16 to where a spacing between the plurality of anchoring elements lies in a range between 100 and 1000 nm (Page 25, lines 5-7).

J) Claim 25

Claim 25 limits claim 16 to where each of the plurality of anchoring elements is embedded into the second functional layer at a depth of between 20 and 500 nm (Page 25, lines 5-7).

K) Claim 26

Claim 26 limits claim 16 to where a thickness of each of the first and the second functional layers lies in a range between 100 and 1000 nm (Page 25, lines 5-7).

L) Claim 27

Claim 27 limits claim 16 to where the intermediate layer comprises a dielectric material (Page 24, lines 1-7).

M) Claim 32

The multilayer semiconductor of independent claim 32 includes a first functional layer 2, a second functional layer 6 coupled to the first functional layer 2, and a plurality of anchoring elements 9 disposed between, and partially embedded in at least one of the first 2 and the second 6 functional layers, where the anchoring elements 9 comprise a different material 4 than that of the first and the second functional layers (Page 19, third paragraph).

N) Claim 33

Claim 33limits claim 32 to further comprising an intermediate layer 1 disposed between the first 2 and the second 6 functional layers, where the plurality of anchoring elements 9 are partially embedded in the intermediate layer 1 (Figures 6-8).

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 16-22, 27 and 32-33 are properly rejected under 35 USC 102(b) as anticipated by Okada et al (Japanese Patent Pub. 2002-158447) and whether claims 23-26 are properly rejected under 35 USC 103(a) as unpatentable over Okada et al.

As noted in the Response to Final Rejection of October 1, 2010 and again in the Statement in Support of Pre-Appeal Brief Request for Review of November 3, 2010, there is no proper Formal statement of Rejection of claims 32 and 33 in the Final Rejection of June 3, 2010.

VII. ARGUMENT

A) THE PRIMARY REFERENCE TO OKADA ET AL DOES NOT DISCLOSE THE SUBJECT MATTER OF INDEPENDENT CLAIMS 16 and 32 AND FURTHER DOES NOT DISCLOSE THE ADDITIONAL SUBJECT MATTER OF DEPENDENT CLAIMS 17-22, 27 and 33.

(1) According to the Final Rejection, with respect to independent claim 16, the Examiner cites on Figure 1 of Okada for disclosing a multilayer semiconductor sensor having a first functional layer (101), a second functional layer 108, an intermediate layer (insulator layer 102 disposed between first functional layer 101 and second functional layer 108. Further according to the rejection, the post 104 is read as the claimed plurality of anchoring elements embedded in at least two of the first 101 and second 108 layers and the intermediate layer 102.

Applicants traverse the rejection because Figure 1 and the supporting disclosure of Okada fail to disclose the layer structure of claim 16 even using the Examiners stated analogy between Figure 1 of Okada and claim 16 claim elements. That is the examiner

is incorrect when asserting that post 104 of Okada are embedded in two of the three layers as required by each of claims 16 and 32. That is post 104 of Okada is only embedded in layer 102 (intermediate layer). The **posts 104 are covered by layer 101** or more particularly sections 107a and are **also covered by solder layer 105 and layer 108**. No definition of "embedded" includes the possibility that posts 104 are embedded in anything other than layer 102. Thus claim 16 is not anticipated as it requires that the anchoring elements (posts) be embedded in at least two layers including the first and second and intermediate layers. When this argument was previously presented by Applicants, the Advisory Action of October 13, 2010 contains an indication by the Examiner that the argument was not persuasive because "the examiner interprets the posts (104), which is present in layer (108) of Okada, as also being embedded in layer (108)." Not only does post fail to be embedded in layer 108 it is also not embedded in anything other than the layer102(intermediate layer).

The Examiner cannot point to any interpretation or definition of "embedded" which could possibly include the "posts 104" of Okada as they are situated in Figure 1 of Okada. That is layer 108 covers the caps 105 which in turn cover the post 104. When the claim calls for anchoring elements to be embedded in one or more layers, it clearly requires some contact between the anchoring elements and the layers. There is not even contact between layer 108 and post 104 much less the embedding of post 104 in layer 108. Furthermore applicants' specification and drawings show and support the proposition that the applicants claimed anchoring elements 9 are embedded in layer 6 and layer 1 in Figure 5. Clearly than the removal of the rejection of claim 16 is in order and is earnestly solicited.

(2) With respect to independent claim 32, essentially the same arguments apply as claim 32 requires "a plurality of anchoring elements disposed between, and partially embedded in at least one of the first and the second functional layers. Therefore because Okada does not disclose that there is any contact between post 104 and layer 108 much less the required "partial embedding", Claim 32 is also clearly patentable over Okada under 35 USC 103.

(3)Dependent claim 17 further limits the structure of claim 16 so that each of the plurality of anchoring elements is embedded in the second functional layer 6 and in the intermediate layer 1 which is also not disclosed by Okada.

(4)Dependent claim 18 limits claim 16 to where a cross-sectional area of each of the plurality of anchoring elements is cylindrical which is also not disclosed by the posts 104 of Okada.

B) DEPENDENT CLAIMS 23-26 DISTINGUISH OVER ANY DISCLOSURE OF OKADA AND THERE HAS BEEN PRESENTED NO PRIMA FACIE CASE FOR THE OBVIOUSNESS OF THE DISTINGUISHING FEATURES

With respect to the rejection of dependent claim 23-26 as being obvious in view of Okada, it is submitted that the Examiner has stated that no effect has been given to the limitation of "semiconductor sensor" of independent claim 1. However this has no bearing on the rejection of the dependent claims which are based on obviousness under

35 USC 103. In that instance, the construction of a semiconductor sensor must carry patentable weight and there is no reason to make the claim limitations concerning the thickness in Okada since it does not disclose a semiconductor sensor. Additionally claims 23-26 contain all the limitations of claim 16 and are also allowable for at least the same reasons as claim 16 discussed above.

CONCLUSION

The withdrawal of the rejections of claims 16-27 and 32-33 and the subsequent allowance of this application are earnestly solicited in view of the foregoing remarks.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-3828 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

**Date: February 23, 2011**

Respectfully Submitted,

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Enclosure:

## VIII. CLAIMS APPENDIX

16. A multilayer semiconductor sensor, comprising:

a first functional layer;

a second functional layer;

an intermediate layer disposed between the first and the second functional layers in a first predetermined region; and

a plurality of anchoring elements each embedded in at least two of the first and the second functional layers and the intermediate layer, where the anchoring elements comprise a different material than that of the first and the second functional layers.

17. The multilayer semiconductor sensor of claim 16, where each of the plurality of anchoring elements is embedded in the second functional layer and in the intermediate layer.

18. The multilayer semiconductor sensor of claim 16, where a cross-sectional area of each of the plurality of anchoring elements is cylindrical.

19. The multilayer semiconductor sensor of claim 16, where a cross-sectional area of each of the plurality of anchoring elements increases from one end of the anchoring element to the other end of the anchoring element.

20. The multilayer semiconductor sensor of claim 16, where a cross-sectional area of each of the plurality of anchoring elements has a conical shape.

21. The multilayer semiconductor sensor of claim 16, where the first and the second functional layers adjoin each other in a second predetermined region that is outside the first predetermined region.

22. The multilayer semiconductor sensor of claim 16, where the intermediate layer is adhered to the first functional layer.

23. The multilayer semiconductor sensor of claim 16, where a diameter of each of the plurality of anchoring elements lies in a range between 100 and 100 nm.

24. The multilayer semiconductor sensor of claim 16, where a spacing between the plurality of anchoring elements lies in a range between 100 and 1000 nm.

25. The multilayer semiconductor sensor of claim 16, where each of the plurality of anchoring elements is embedded into the second functional layer at a depth of between 20 and 500 nm.

26. The multilayer semiconductor sensor of claim 16, where a thickness of each of the first and the second functional layers lies in a range between 100 and 1000 nm.

27. The multilayer semiconductor sensor of claim 16, where the intermediate layer comprises a dielectric material.

32. A multilayer semiconductor, comprising:

a first functional layer;

a second functional layer coupled to the first functional layer; and

a plurality of anchoring elements disposed between, and partially embedded in at least one of the first and the second functional layers, where the anchoring elements comprise a different material than that of the first and the second functional layers.

33. The multilayer semiconductor of claim 32, further comprising an intermediate layer disposed between the first and the second functional layers, where the plurality of anchoring elements are partially embedded in the intermediate layer.

## IX. EVIDENCE APPENDIX

(None)

X. RELATED PROCEEDINGS APPENDIX
(None)